

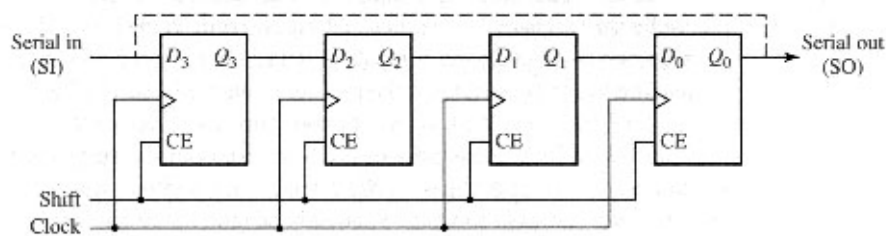
Computer Organization & Architecture

Lecture #5

Shift Register

A shift register is a register in which binary data can be stored and then shifted left or right when a shift signal is applied. Bits shifted out one end of the register may be either lost or shifted back in on the other end.

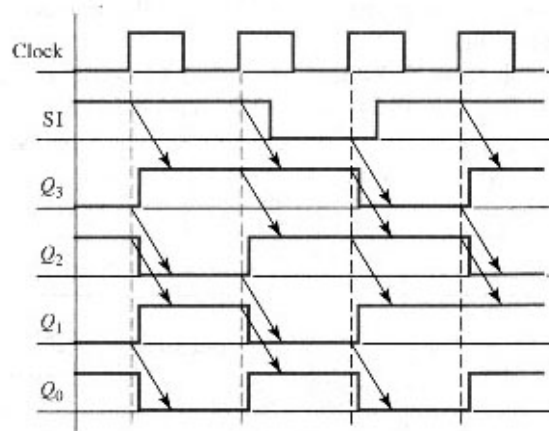
Shown below is a 4-bit shift register with serial input and serial output constructed of D-CE flip-flops.



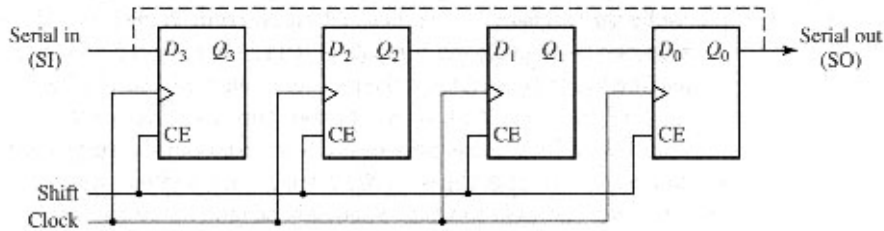
When Shift = 1, the clock is enabled and shifting occurs on the rising clock edge. When Shift = 0, no shifting occurs and the data in the register remains unchanged.

The serial input (SI) is loaded into the first flip-flop (Q_3) by the rising edge of the clock. At the same time, the output of the first flip-flop is loaded into the second flip-flop, the output of the second flip-flop is loaded into the third flip-flop, and the output of the third flip-flop is loaded into the last flip-flop. Because of the propagation delay of the flip-flops, the output value loaded into each flip-flop is the value before the rising clock edge.

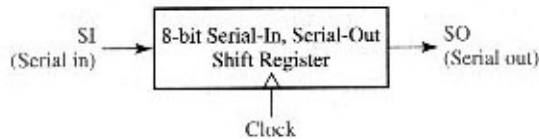
Shown below is a shift register timing diagram where the shift register initially contains the value 0101 and the serial input sequence is (last) 1, 1, 0, 1 (first).



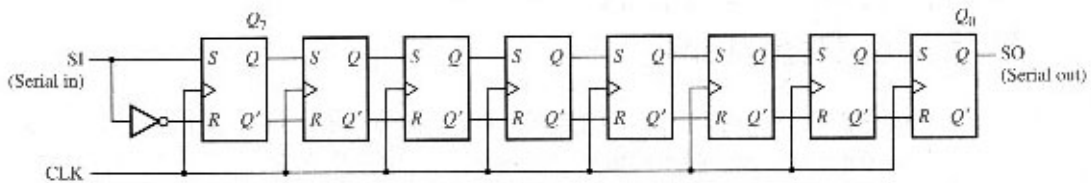
If the serial output is connected back to the serial input the shift register performs an end-around shift. If the initial contents of the register is 0111: after one clock cycle the contents is 1011; after two clock cycles the contents is 1101; after three clock cycles the contents is 1110; after four clock cycles the contents is 0111, the same as the initial contents.



Shift registers with 4, 8, or more flip-flops are available in integrated circuit form. Shown below is the block diagram for an 8-bit serial-in, serial-out shift register.

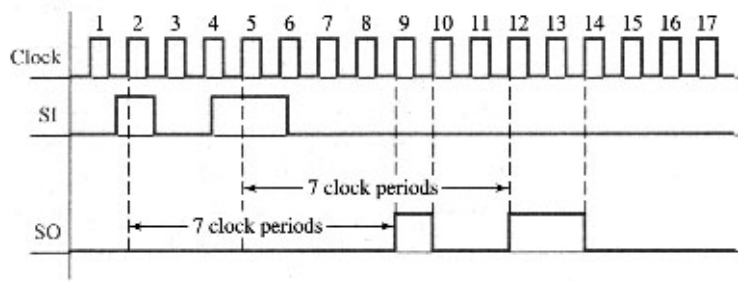


Shown below is the circuit diagram for an 8-bit serial-in, serial-out shift register constructed of S-R flip-flops.

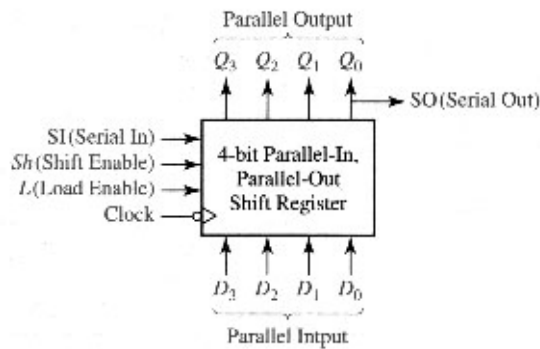


Serial in implies that data is shifted into the first flip-flop one bit at a time, and the flip-flops cannot be loaded in parallel. Serial out implies that data can only be read out of the last flip-flop and the outputs from the other flip-flops are not connected to terminals of the integrated circuit. The flip-flop inputs are $S = SI$ and $R = (SI)'$. If $SI = 1$, a 1 is shifted into the register when it is clocked, and if $SI = 0$, a 0 is shifted in.

Shown below is a timing diagram for the 8-bit serial-in, serial-out shift register.



Shown below is a block diagram for a 4-bit parallel-in, parallel-out shift register.



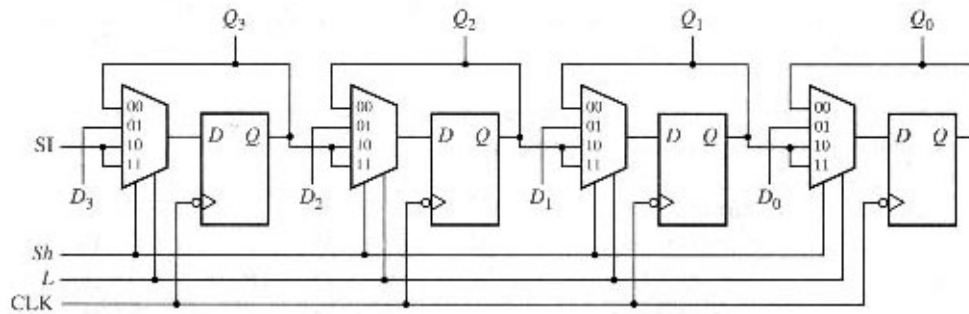
Parallel-in implies that all four input bits can be loaded at the same time, and parallel-out implies that all four output bits can be read out at the same time.

The shift register has two control inputs, shift enable (Sh) and load enable (L). The table below describes how these inputs are used to control the shift register.

Inputs		Next State				Action
Sh (shift)	L (load)	Q3+	Q2+	Q1+	Q0+	
0	0	Q3	Q2	Q1	Q0	No Change
0	1	D3	D2	D1	D0	Parallel Load
1	X	SI	Q3	Q2	Q1	Serial Right Shift

All state changes occur immediately following the falling edge of the clock.

Shown below is the circuit diagram for a 4-bit parallel-in, parallel-out shift register constructed of D flip-flops and multiplexers.



When $Sh = L = 0$, the flip-flop Q_3 output is selected by the MUX, so $Q_{3+} = Q_3$ and no state change occurs. When $Sh = 0$ and $L = 1$, the data input D_3 is selected and loaded into the flip-flop. When $Sh = 1$ and $L = 0$ or 1 , SI is selected and loaded into the flip-flop. The other multiplexers act the exact same way for their corresponding flip-flops.

The next-state equations for the flip-flops are:

$$Q_{3+} = (Sh)'L'(Q_3) + (Sh)'L(D_3) + Sh(SI)$$

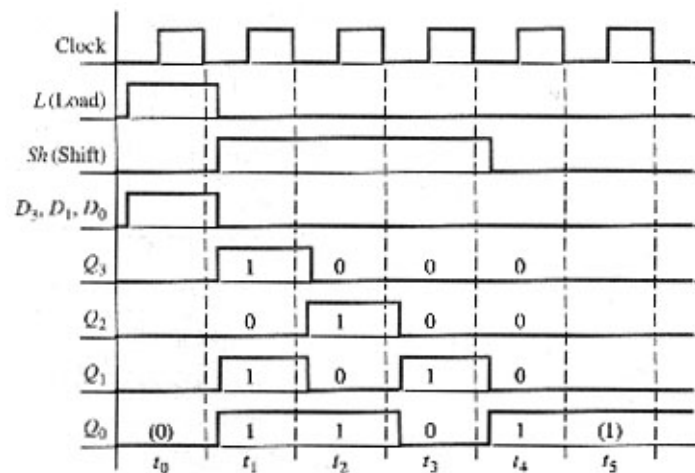
$$Q_{2+} = (Sh)'L'(Q_2) + (Sh)'L(D_2) + Sh(Q_3)$$

$$Q_{1+} = (Sh)'L'(Q_1) + (Sh)'L(D_1) + Sh(Q_2)$$

$$Q_{0+} = (Sh)'L'(Q_0) + (Sh)'L(D_0) + Sh(Q_1)$$

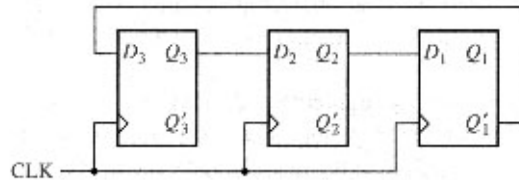
A typical application of this register is the conversion of parallel data to serial data or serial data to parallel data. The output of the last flip-flop (Q_0) serves as a serial output as well as one of the parallel outputs.

Shown below is a timing diagram for a 4-bit parallel-in, parallel-out shift register.



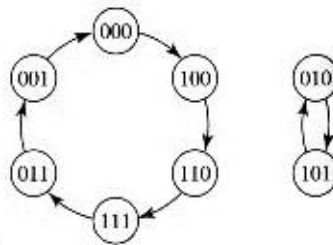
The timing diagram assumes that the register is initially clear ($Q_3Q_2Q_1Q_0 = 0000$), and that the serial input is $SI = 0$ throughout, and that the data inputs $D_3D_2D_1D_0$ are 1011 during the load time.

Shown below is the circuit diagram for a 3-bit shift register constructed of D flip-flops.



Notice that the complemented output of the last flip-flop is fed back to the input of the first flip-flop. If the initial state of the register is 000, then the initial input value of D_3 is 1, so then after the first clock pulse the register state is 100.

Shown below are the state graphs for the 3-bit shift register.



If the initial state of the register is either: 000, 100, 110, 111, 011, or 001 then the graph on the left shows the next-state sequence for the register. If the initial state of the register is either: 010 or 101 then the graph on the right shows the next-state sequence for the register.

A circuit that cycles through a fixed sequence of states is called a counter, and a shift register with inverted feed back is often called a Johnson counter.